CS 250 2017 Spring Practice Midterm Exam 01

Purdue University

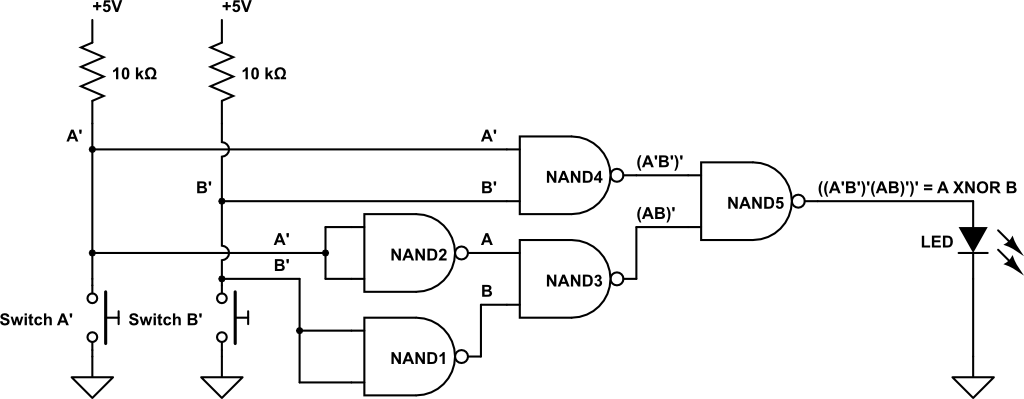
1. Technology change is a significant concern of computer designers and programmers.
   1. True – Yes because technology is always improving
   2. False
2. The bit string 01001001 has no meaning.
   1. True – **A Bit string has no meaning until we give it one**
   2. False –
3. The sum of products form of the row A=0 and B=1 for the truth table of the two-input exclusive-OR function is A XOR B.
   1. True
   2. False –**SOP requires use of AND**
4. Consider this Karnaugh map for inputs X, Y, and Z.

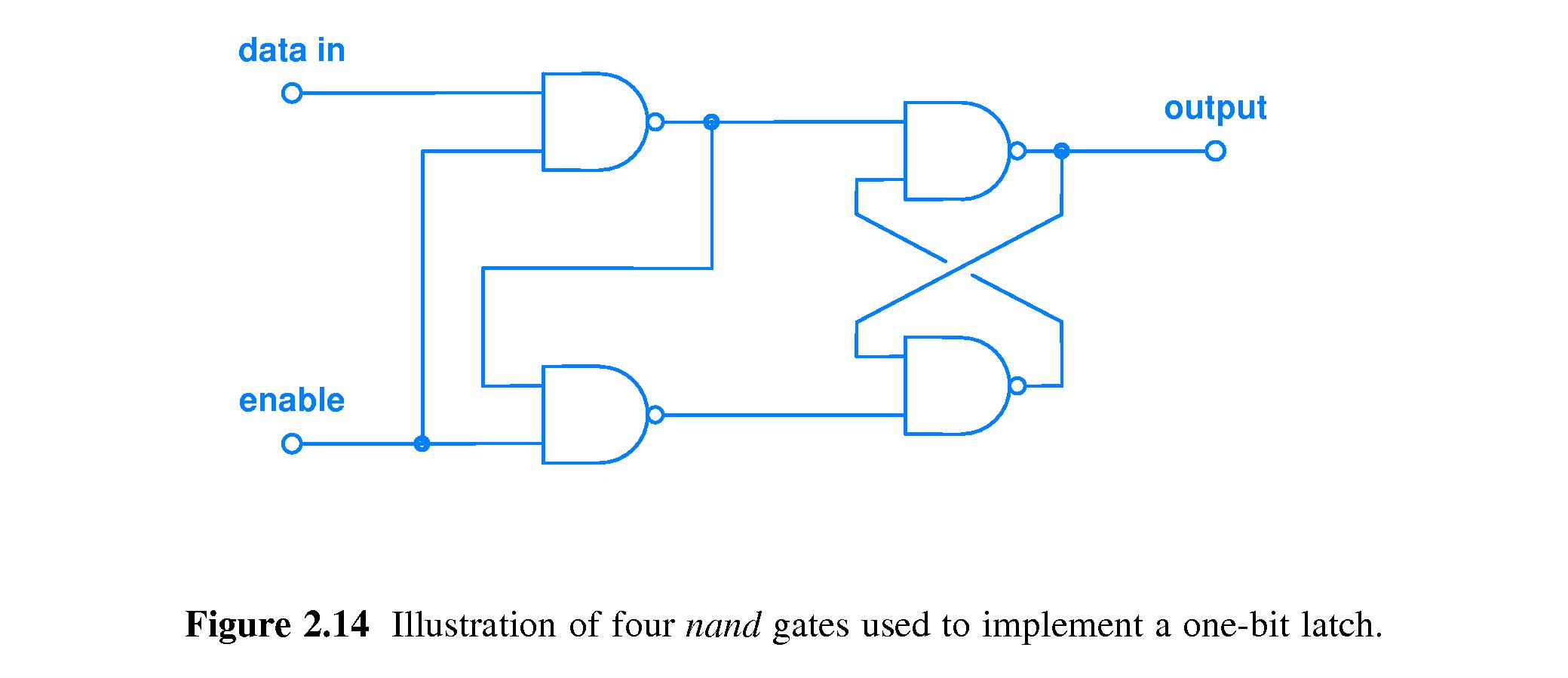
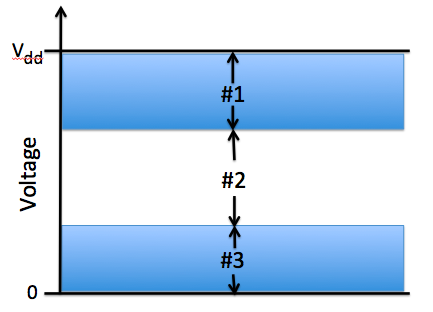
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| f(X,Y,Z) | XY = 00 | XY = 01 | XY = 11 | XY =10 |
| Z = 0 | 1 | 0 | 0 | 1 |
| Z = 1 | 1 | 0 | 1 | 1 |

Assume that you have access only to X, Y, and Z, so if you want Z’, your circuit must compute it. A minimal sum of products circuit to implement this truth table has

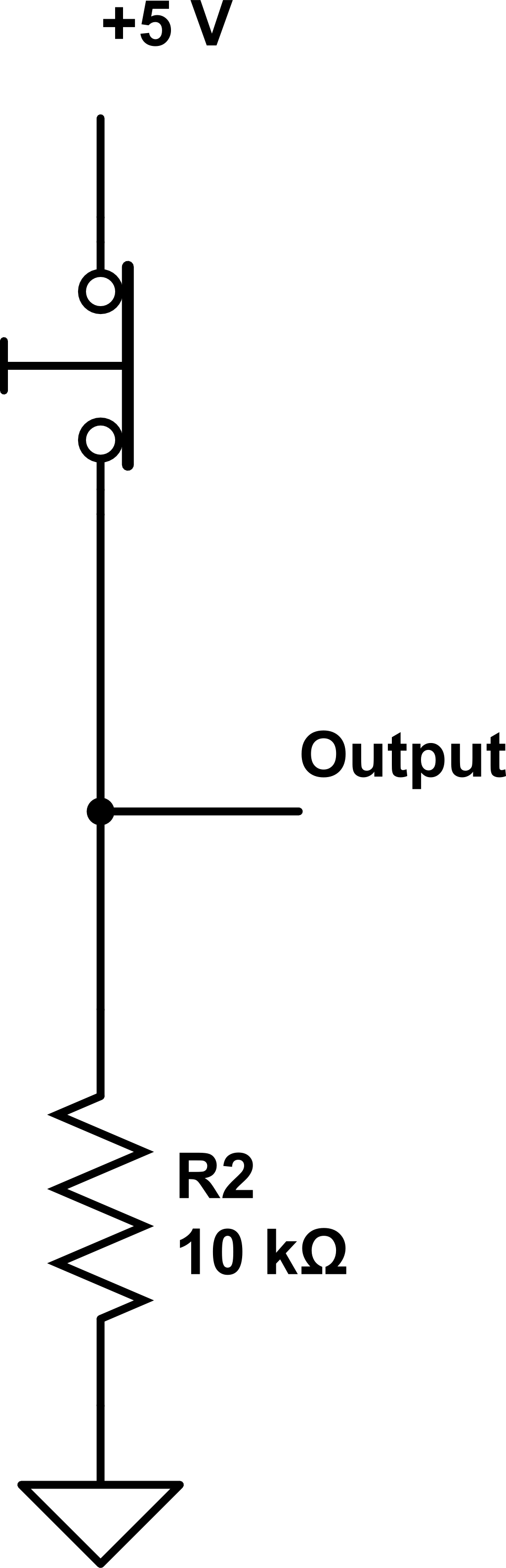
* 1. Two two-input NAND gates and a two-intput NOR gate
  2. One two-input AND gate, one two-input OR gate, and one NOT gate - The SOP is Y’ + XZ
  3. One four-input NAND gate and an inverter
  4. Five two-input NAND gates
  5. None of the above answers is correct

1. When software would use iteration to carry out a repetitive task, hardware uses
   1. An increase in supply voltage
   2. Replication – This way it can replicate the output over and over.
   3. Higher speed gates
   4. Exclusive-Or gates
   5. None of the above
2. To point to one of 32 locations requires
   1. A multiplexer
   2. A 5-bit string – **2^5 locations can be pointed to. C and D can point to more than 32 which is excessive.**
   3. A 32-bit pointer
   4. A decoder with 32 inputs
   5. None of the above is necessary
3. The truth table for a 4-bit adder made from full adders has how many rows?
   1. 4
   2. 16
   3. 256
   4. 2256
   5. None of the above – It would be 4 bits addend and 4 bits augend plus a carry in so it would be 2^9= 512
4. Which adder circuit type can be operated the fastest assuming that all gate delays are equal and all wire propagation delays are equal?
   1. 1’s complement – This is faster because it doesn’t have to add the extra 1.
   2. 2’s complement - **2’s complement avoids the end around carry required of 1’s complement**
   3. 1’s and 2’s complement are equally fast
   4. Because 1's complement is faster than 2’s complement for some (addend, augend) pairs and not for other pairs, it is incorrect to say that one of these adder types can be operated faster than the other.
   5. None of the above answers is correct.
5. Which of the following expressions and notations represents or corresponds to the most negative value possible for an 8-bit 2’s complement number?
   1. 11111111 xThis is -1
   2. 0x80 – **would be 1000 0000 which in 2’s complement is -128**
   3. – (27 – 1) x this is -127
   4. – (28 – 1) x this is more than 8 bits
   5. None of the above answers is correct
6. The bit string 1001000000010101 could be a packed BCD value.
   1. True – It would be 9 0 1 5
   2. False

Consider the circuit below, which was constructed for Lab 01, when answering the two questions that follow.  
  


1. The operation of this circuit will be unchanged if a 2-input NOR gate is substituted for NAND1 and no other change is made.
   1. True – Because it would still work as an inverter for input B.
   2. False
2. The operation of this circuit will be unchanged if the 10 kΩ resistors are replaced with zero ohm resistors.
   1. True
   2. False – There needs to be resistors otherwise it will not be active low.
3. Consider Figure 2.14 from the textbook.  
     
   Let t be the initial time this circuit is examined. Which statement is true?
   1. If at time t enable = 1 and data in = 0 and are held constant, then output(t) = 0 and output(t+1) = 0 FALSE we do not know what output(t) would be
   2. If at time t enable = 1 and data in = 0 and are held constant, then output(t) = X and output(t+1) = 1 **FALSE output(t+1) should be 0**
   3. If at time t enable = 0 and data in = 1 and are held constant, then output(t) = X and output(t+1) = 1 FALSE output(t+1) would be output(t)
   4. None of the statements A, B, and C are true **The rest are false**
4. For 8-bit sign-magnitude and 1’s complement representations of the decimal value -3, in how many bit positions do these two representations differ?
   1. 1 magnitude – 1000 0011
   2. 3 1’s comp – 1111 1100
   3. 5
   4. 7 – The difference between the two would be all but the first bit.
   5. None of the above
5. A digital logic circuit that given an input bit string X computes an output Y and then, later, given the same input bit string X computes a different output Z must contain
   1. A counter
   2. A NOT gate
   3. A latch – Depending on the last input the latch can change the output **because it is a sequential circuit.**
   4. An adder
   5. A decoder
6. A function in a program produces a result only after it has been called. Hardware, upon receiving power, produces an output signal immediately and at all time thereafter, no matter how many gate delays circuit input signals must propagate through on the longest path to a circuit output.
   1. True – Hardware starts running instantly
   2. False
7. What fraction of the possible input values yield Sum = 0 and Carry out = 1 for a full adder?
   1. 1/8
   2. 2/4
   3. 3/8 – **It would be 011, 101, 110**
   4. 4/16
   5. 5/8
8. 24 bytes is 4 times as many bytes as is 20 (base 16) bits.
   1. True - **24 bytes = 24 x 23 bits = 27 bits. 20 base 16 = 2x161+0x160 = 32 = 25. The ratio of 27 to 25 is 22 = 4.**
   2. False
9. Which of the following is one of DeMorgan’s Laws?
   1. (X’)’ = X
   2. (AB)’ = A’ + B’ - **TRUE**
   3. (C’D’) = C’ + D’
   4. (Y + Z)’ = Y’ + Z’
   5. None of the above is one of DeMorgan’s Laws
10. Memory locations are pointed to by hardware. Designing a computer with four times more memory than specified in the original design requires
    1. Using one more address bit
    2. Using two more address bits - **Each additional address bit doubles the number of locations that can be pointed to.**
    3. Using four more address bits
    4. Using four times the number of address bits
    5. None of the above
11. Consider the following diagram showing three voltage bands labeled #1, #2, and #3.  
      
      
    Which band, or which combination of bands, guides us in designing digital computer circuits where the logic gate input signal voltage levels need not be perfect yet gate operation will be digital, not analog?
    1. #1
    2. #1 and #2
    3. #2
    4. #2 and #3
    5. None of the above answers is correct – It is 1 and 3 because the blue area is the acceptable range of voltage

|  |  |  |
| --- | --- | --- |
| A | B | f(A,B) |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

1. Consider the following truth table.  
     
     
     
     
     
     
     
   The missing truth table entries, in order from top to bottom, could be
   1. 0 0 1 0 if f(A,B) = (A + B) modulo 2
   2. 0 1 1 0 if f(A,B) = A XNOR B – FALSE would be A XOR B
   3. 1 0 0 0 if f(A,B) corresponds to a universal logic gate – would be A NOR B which is universal because it can do NOT,OR, AND
   4. 0 0 0 1 if f(A,B) corresponds to a universal logic gate – FALSE would be A AND B which is not universal
   5. X 1 0 X if f(A,B) = A’
2. The binary string 1010, when interpreted as a 2’s complement number represents the decimal number value Subtract 1: 1001 Flip Bits: 0110
   1. 10
   2. -2
   3. -5
   4. -6 – Because it starts with 1 which is negative and then when converted to unsigned is equal to 6
   5. None of the above
3. Consider this circuit to generate a digital input.  
     
     
   1. This input circuit is an active low design – TRUE because when the switch is active it removes connection to power and thus it is active low
   2. We cannot say whether this input circuit is active high or not until information about whether the switch is being pushed is given to us
   3. This circuit will work only when we exchange the positions of the switch and the resistor in the circuit, that is, put the switch where the resistor is shown and put the resistor where the switch is shown
   4. This design would be improved if R2 had the value 470 ohms
   5. None of the above is correct.
4. The reason we prefer to build digital logic circuits to operate in base 2 rather than base 10 is
   1. Cost
   2. Speed
   3. Easier to manufacture
   4. Any of the above – Its easier, faster, and cheaper
   5. None of the above
5. Each possible combination of inputs is applied to both a 2-input NAND gate and a 2-input XOR gate, and the outputs of the two gates are compared. How many times will the outputs of these two gates be the same? NAND: 1110 XOR: 0110

A 0 B 1 C 2 D 3 – for 01, 10, 11 E 4

1. The amount of time needed by a combinatorial circuit to complete its computation is
   1. measured in units of gate delays. – That’s just how it is measured
   2. essentially zero because logic gates produce an output voltage as soon as they receive power.
   3. is unpredictable.
   4. Is all of the above answers
   5. is none of the above answers.
2. Fill in the table to show how the following 32-bit binary string (byte boundaries are indicated by space for convenience) 00001111 10101100 11110000 10011010  
   will be stored in computer memory assuming Little Endian byte order.

|  |  |
| --- | --- |
| Addressable Memory Location Number | Little Endian Solution (least significant byte goes into the lowest memory address) |
| *k* | 10011010 |
| *k* + 1 | 11110000 |
| *k* + 2 | 10101100 |
| *k* + 3 | 00001111 |

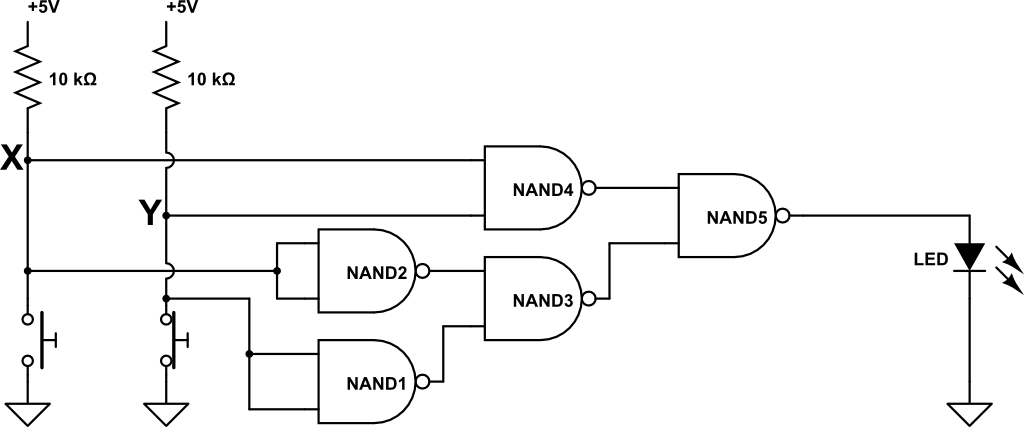
1. Why is a biased exponent representation used by the IEEE Floating Point Standard?  
   In order to differentiate between positive and negative

**It makes alignment of mantissas easy because the bias translates the allowed range of positive and negative exponent values to the same range of unsigned (i.e., positive) integers, thereby translating the comparison of two exponents into a comparison of two unsigned integers, an easier comparison than comparing signed numbers.**

1. In Figure 2.3 of the textbook, which transistor turns on when the input is a low voltage?  
   The transistor connected to ground.
2. The 4-bit unsigned integers 1010 and 0110 are added. What should be the output of a well-designed ALU?

The output would be 0000 and **an overflow signal**

1. Draw a voltage waveform that has one falling edge.
2. Consider the schematic below for the following questions.



* 1. Using the given names of any relevant signals shown in the schematic, what is the Boolean expression for the output of gate NAND4?

(XY’)’

* 1. Is the LED **on** or **off** or **cannot determine with the given information**?

It is off because NAND 5 produces an output of 0 when X is 1 and Y is 0.

1. What principle allows for the simplification of descriptions of hardware by omission of unimportant detail? Abstraction